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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/099,883	03/14/2002	John H. Oates	0102323-00099	5431
21125	7590	07/12/2005	EXAMINER	
NUTTER MCCLENNEN & FISH LLP WORLD TRADE CENTER WEST 155 SEAPORT BOULEVARD BOSTON, MA 02210-2604			VLAHOS, SOPHIA	
			ART UNIT	PAPER NUMBER
			2637	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/099,883	Applicant(s) OATES ET AL.	
	Examiner SOPHIA VLAHOS	Art Unit 2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 March 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 and 15 is/are rejected.
- 7) ☒ Claim(s) 13 and 14 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on 3/14/2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

The specification refers to base station as block "100" and the rake modems as block "102" respectively. Figure 1 designates the rake modem as "100" and the base station as "112". It is recommended to modify either the specification or Figure 1.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1,4,7 are rejected under 35 U.S.C. 102(a) as being anticipated by Hottinen et al. (U.S. 6,449,266).

With respect to claim 1, Hottinen et al., disclose a first processing element (Fig. 7, elements 80-83) which generates a matrix (hereinafter "gamma matrix") representing a correlation between a code associated with one user and those associated with one or more other users (column 9, line 20, column 11, lines 11-18).

A set of one or more second processing elements coupled with the first processing element (Fig. 8, element 62) the set of processing elements generating a matrix (hereinafter "R-matrix") representing cross-

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correlations among user waveforms (Fig.8, element 73, column 8, lines 14-39).

A third processing element coupled with the set of processing elements, the further processing element generates symbol estimates (Fig.6, elements 63a-63c, column 11, lines 38-39).

With respect to claim 4, all the limitations of claim 1 were disclosed above by Hottinen et al., (U.S. 6,449,266). Hottinen et al., disclose a host controller coupled to each of the set of second processing elements (Fig. 8, element 55), the host controller generates a partitioning of the R-matrix (Fig.8, element 74), that partitioning divides the R-matrix into one or more portions based on a number of users and a number of available second processing elements (column 11, lines 45-52).

The host controller assigns to each second processing element within the set of second processing elements a portion of the R-matrix to generate according to the partitioning (Fig. 8, column 11, lines 25-29, 45-52).

Each one of the set of second processing elements generates the assigned portion of the R-matrix according to the partitioning (Fig. 8, column 11, lines 25-29).

The host re-calculates the partitioning of the R-matrix when a user is added or removed from the spread spectrum system, and assigns a new

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portion of the R-matrix to each second processing element within the set of second processing elements according to that new partitioning (column 11, lines 39-52).

With respect to claim 7, all the limitations of claim 1 were disclosed above by Hottinen et al., (U.S. 6,449,266). Hottinen discloses a host controller coupled with the first processing element, the set of processing elements, and the further processing element (Fig.6, element 55). The host controller synchronizes data flow between the first processing element and the set of second processing elements (column 11, lines 25-29), the host controller synchronizes data flow between the set of second processing elements and the third processing element (Fig. 6, element 55).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 2,3,5,6,8-12,15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hottinen et al., (U.S. 6,449,266) in view of Hetz et. al (U.S. 5,917,829).

With respect to claim 2, Hottinen et al., (U.S. 6,449,266) disclose all the limitations of claim 2 except a memory that is coupled to the first processing element and the set of the second processing elements. The first processing element placing the gamma matrix in the memory for access by the set of second processing elements.

In the same field of endeavor, however, Hertz et. al (U.S. 5,917,829) discloses a memory (Fig. 4, elements 33,34,35, column 12, lines 1-5) that is coupled to the first processing element and the set of second processing elements. Hertz et al., also disclose the first processing element placing the gamma matrix in the memory for access by the second processing elements. (Fig. 4, column 11, lines 55-60).

It would have been obvious to one of ordinary skill in the art at the time of the applicants invention to modify Hottinen et al., by incorporating Hertz et al.'s memory and the first processing element placing the gamma matrix in the memory for access by the second processing elements, because it yields detected information with low BER at a relatively small computational effort (Hertz et al., column 3, lines 1-2).

Regarding claim 3, Hottinen et al., discloses all the limitations of claim 3 except a multi-port data switch coupled to the first processing element and to the memory. The first processing element places the gamma matrix in

the memory via the data switch. Hetz et al (U.S. 5,917,829) discloses a multi-port data switch coupled to the first processing element and to the memory (column 11, lines 51-60). Hertz et al., disclose the above limitation without using the term "multi-port data switch", instead the terms "bus line" (column 11, line 56) and "each value of the matrix is directly fed..." (column 12, lines 56-60) are used and they can inherently function as a multi-port data switch. The first processing element places the gamma matrix in the memory via the data switch (column 11, lines 51-60). It would have been obvious to one of ordinary skill in the art at the time of the applicants invention to modify Hottinen et al., by incorporating Hertz et al. because it yields detected information with low BER at a relatively small computational effort (Hertz et al., column 3, lines 1-2).

With respect to claim 5, Hottinen et al., disclose all the limitations of claim 5 except a memory that is coupled to each of the processing elements in the set of second processing elements and the third processing element, and the set of second processing elements each placing its respective portion of the R-matrix in the memory for access by the third processing element. Hertz et al., disclose the above limitations (Fig. 4, column 11, lines 51-60). It would have been obvious to one of ordinary skill in the art at the time of the applicants invention to modify Hottinen et al., by incorporating Hertz et al. because it yields detected information with low

BER at a relatively small computational effort (Hertz et al., column 3, lines 1-2).

With respect to claim 6, Hottinen et al., discloses all the limitations of claim 6, except a multi-port data switch coupled to each of the processing elements in the set of processing elements and to the memory, and each of the set of second processing elements placing its respective portion of the R-matrix in the memory via data switch. Hertz et al., disclose the above limitations (Fig.4, column 11, lines 51-60). It would have been obvious to one of ordinary skill in the art at the time of the applicants invention to modify Hottinen et al., by incorporating Hertz et al. because it yields detected information with low BER at a relatively small computational effort (Hertz et al., column 3, lines 1-2).

With respect to claim 8, Hottinen et al disclose a first element (Fig. 7, elements 80-83) which generates a matrix (hereinafter "gamma matrix") representing a correlation between a code associated with one user and those associated with one or more other users (column 9, line 20, column 11, lines 11-18).

A set of one or more second processing elements (Fig. 8, element 62) each of the processing elements within the set generates a portion of a matrix (hereinafter "R-matrix") representing cross-correlations among user waveforms (Fig.8, element 73, column 8, lines 14-39).

A third processing element the further processing element generates symbol estimates (Fig.6, elements 63a-63c, column 11, lines 38-39).

While Hottinen et al., are silent about a first processing element coupled with a multi-port data switch, a set of one or more second processing elements coupled with the multi-port data switch, a third processing element coupled with the multi-port data switch. Hetz et. al (U.S. 5,917,829) discloses a multi-port data switch coupled to the first processing element and to the memory (column 11, lines 51-60). Hertz et al., disclose the above limitation without using the term "multi-port data switch", instead the terms "bus line" (column 11, line 56) and "each value of the matrix is directly fed..." (column 12, lines 56-60) are used and they can inherently function as a multi-port data switch.

It would have been obvious to one of ordinary skill in the art at the time of the applicants invention to modify Hottinen et al., by incorporating Hertz et al. because it yields detected information with low BER at a relatively small computational effort (Hertz et al., column 3, lines 1-2).

With respect to claim 9, Hottinen et al., disclose a host controller generating a partitioning of the R-matrix wherein the R-matrix is divided by the partitioning into one or more portions (Fig.8, element 74, column 11, lines 45-52). The host controller synchronizing the generation of the R-

matrix on the set of second processing elements such that each of the second processing elements within the set generates a portion of the R-matrix according to the partitioning (column 11, lines 25-29, 45-52).

While Hottinen et al., are silent about the host controller coupled with the multi-port data switch and each of the second processing elements within the set coupled to the multi-port data switch, the second processing elements each placing its respective portion of the R-matrix in memory accessible by the third processing element. Hertz et al., (U.S. 5,917,829) Discloses the above limitations (column 11, lines 51-60, column 12, lines 1-5). It would have been obvious to one of ordinary skill in the art at the time of the applicants invention to modify Hottinen et al., by incorporating Hertz et al. because it yields detected information with low BER at a relatively small computational effort (Hertz et al., column 3, lines 1-2).

With respect to claim 10 Hottinen et al., disclose the host controller generating a new partitioning when a user is added or removed from the spread spectrum system (column 11, lines 45-52) and the set of second processors generating the portions of the R-matrix according to the new partitioning (column 11, lines 45-51).

With respect to claim 11 Hottinen et al., disclose the first processor updating the gamma matrix to reflect the addition or removal of a user from the system (Fig. 6, element 55, column 10, lines 50-63). While

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Hottinen is silent about a memory coupled with the first processing element and the set of second processing elements and the first processor placing in the memory the gamma matrix. Hertz et al., discloses the limitation a memory coupled with the first processing element and the set of second processing elements (column 12, lines 1-5) and the first processor placing in the memory the gamma matrix (column 12, lines 56-60). It would have been obvious to one of ordinary skill in the art at the time of the applicants invention to modify Hottinen et al., by incorporating Hertz et al. because it yields detected information with low BER at a relatively small computational effort (Hertz et al., column 3, lines 1-2).

Regarding claim 12, Hottinen et al., disclose all the limitations of claim 12 except for a memory coupled with the set of second processing elements and the third processing element, the set of second processing elements placing in the memory the portion of the R-matrix. Hertz et al., disclose the above limitations (column 12, lines 1-5, column 11, lines 56-60) It would have been obvious to one of ordinary skill in the art at the time of the applicants invention to modify Hottinen et al., by incorporating Hertz et al. because it yields detected information with low BER at a relatively small computational effort (Hertz et al., column 3, lines 1-2).

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With respect to claim 15, Hottinen et al., disclose the third processing element generates the symbol estimates based on a composition of the R-matrix (column 11, lines 38-44).

Allowable Subject Matter

5. Claims 13,14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

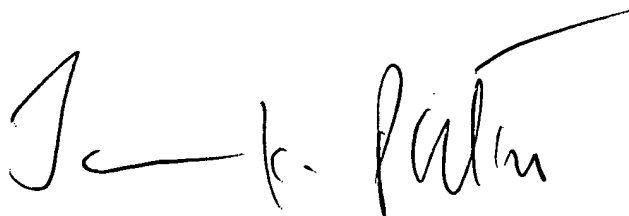
Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JAY PATEL can be reached on 571 272 2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SV
July 8, 2005

A handwritten signature in black ink, appearing to read "J. K. Patel", with a long horizontal stroke extending from the end of the name.

JAY K. PATEL
SUPERVISORY PATENT EXAMINER